

INHERENTLY STOCHASTIC SPIKING NEURONS FOR PROBABILISTIC NEURAL COMPUTATION

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Abstract

We propose a new memristive neuron circuit that follows the stochastic spike response model (SRM) and can be used for spike-based probabilistic algorithms. We show that the switching of the memristor is akin to the stochastic firing of the SRM. The analysis and simulations confirm that the proposed neuron circuit satisfies the *neural computability condition* that enables probabilistic neural sampling and spike-based Bayesian learning and inference algorithms.

Motivation

- Recent theoretical studies have shown that probabilistic spiking can be interpreted as inference and learning in cortical microcircuits.
- The research on systems that use noise as a computational resource has become a rapidly growing field [1].
- However, such systems have two critical requirements: (i) the neurons should follow a specific model, and (ii) stochastic spiking should be implemented efficiently for it to be scalable.
- We propose to use the inherent randomness of nano-scale memristors [2] for implementing stochastically spiking neurons that fulfill both requirements [3].

Notation

Parameter	Description
R_{on} and R_{off}	Low and high resistances of the memristor
τ_0	Average switching time for a device under $V = 0$
V_0	Memristive switching voltage sensitivity

Stochastic Model of the Memristor

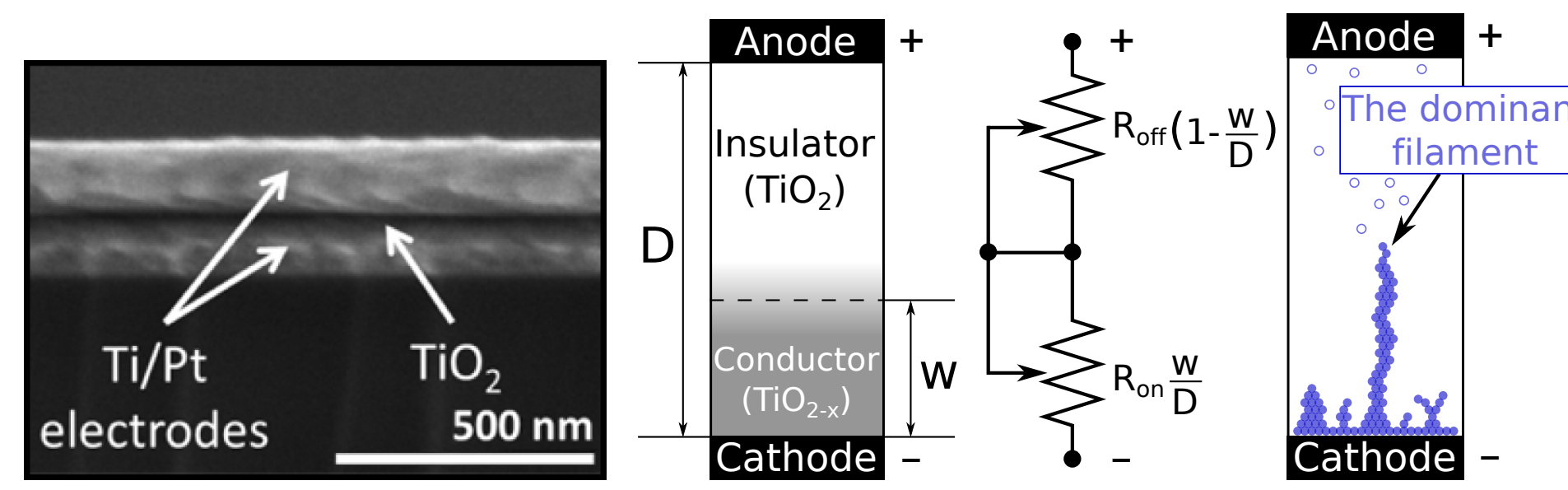


Figure 1 : Memristor, the barrier and filament models.

To account for stochastic filament formation, we propose a simple enhanced memristor model:

$$\begin{cases} I = g_m \left(\frac{w}{D} \right) V, & \text{where } g_m \left(\frac{w}{D} \right) = \left(R_{off} - \Delta R \frac{w}{D} \right)^{-1}, \\ dw = \underbrace{f(w, V) dt}_{\text{deterministic term}} + \underbrace{(\theta(V) \cdot D - w) dN(\tau)}_{\text{stochastic term}}, \end{cases}$$

where the stochastic term follows the dynamics of an inhomogeneous Poisson process $dN(\tau)$ with a time constant that exponentially depends on applied voltage:

$$\tau(V) = \tau_0 \exp(-V/V_0),$$

where τ_0 and V_0 are parameters of the appropriate units. This leads to the following dynamics:

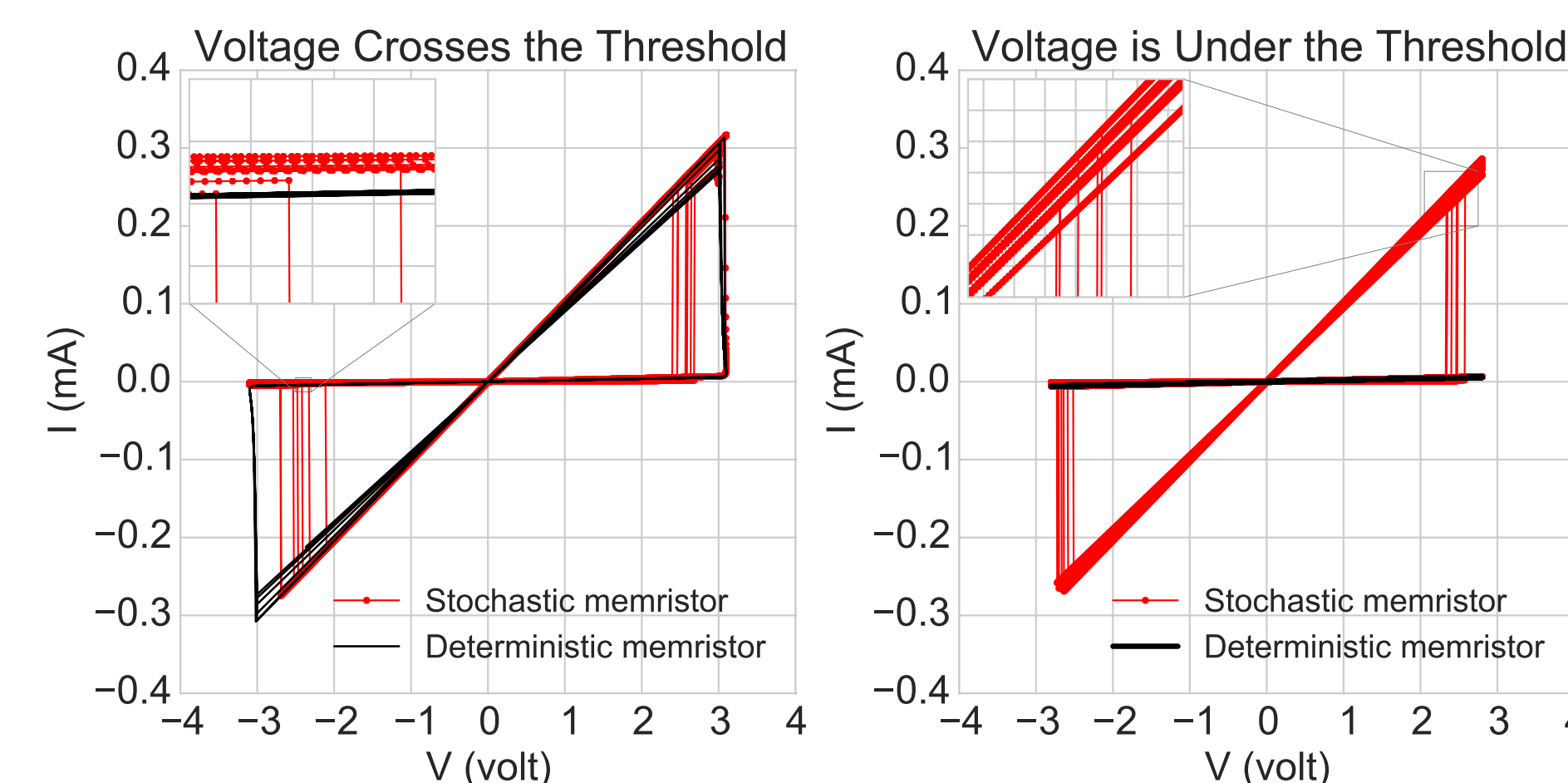


Figure 2 : Deterministic and stochastic I-V curves.

Probabilistically Firing Neuron

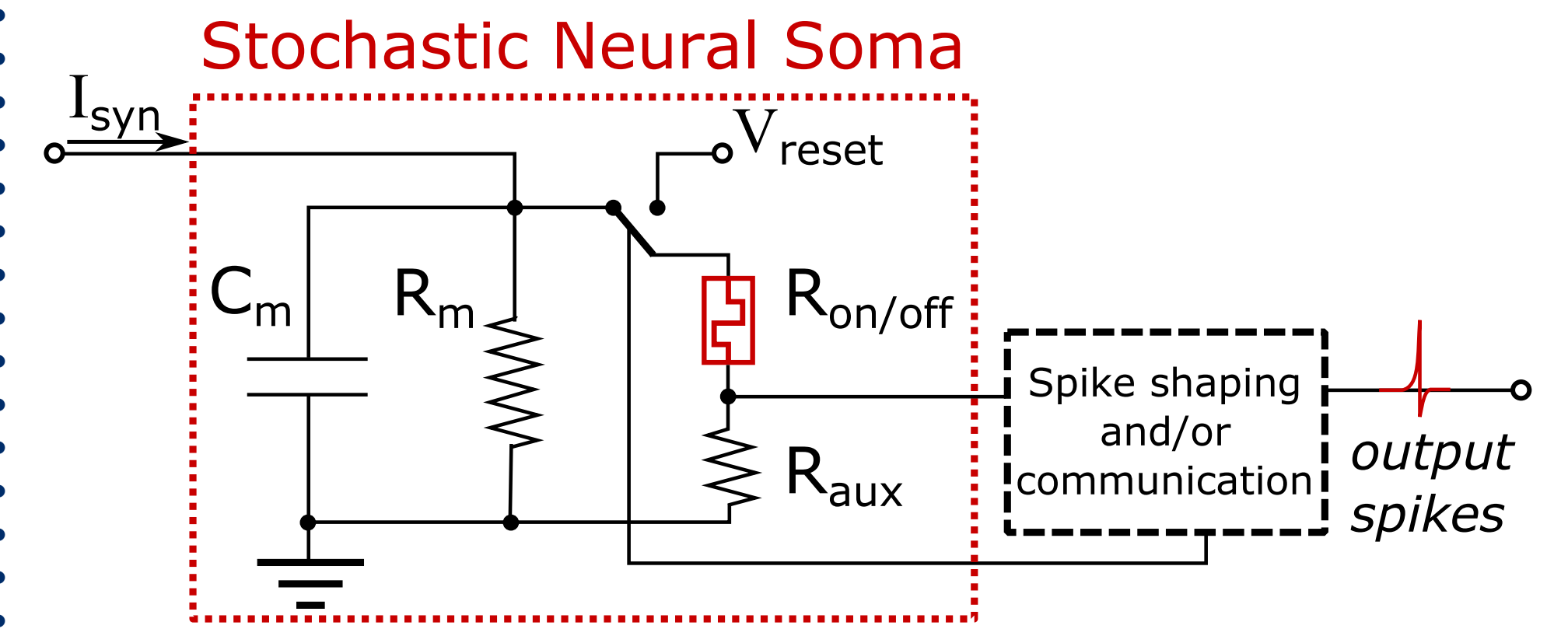


Figure 3 : Memristive neuron circuit.

- Each switching event generated by the memristor is converted into an analog or a digital spike.
- The circuit was simulated for constant noisy input synaptic currents. Spiking statistics and the power dissipation on the memristor are presented below.

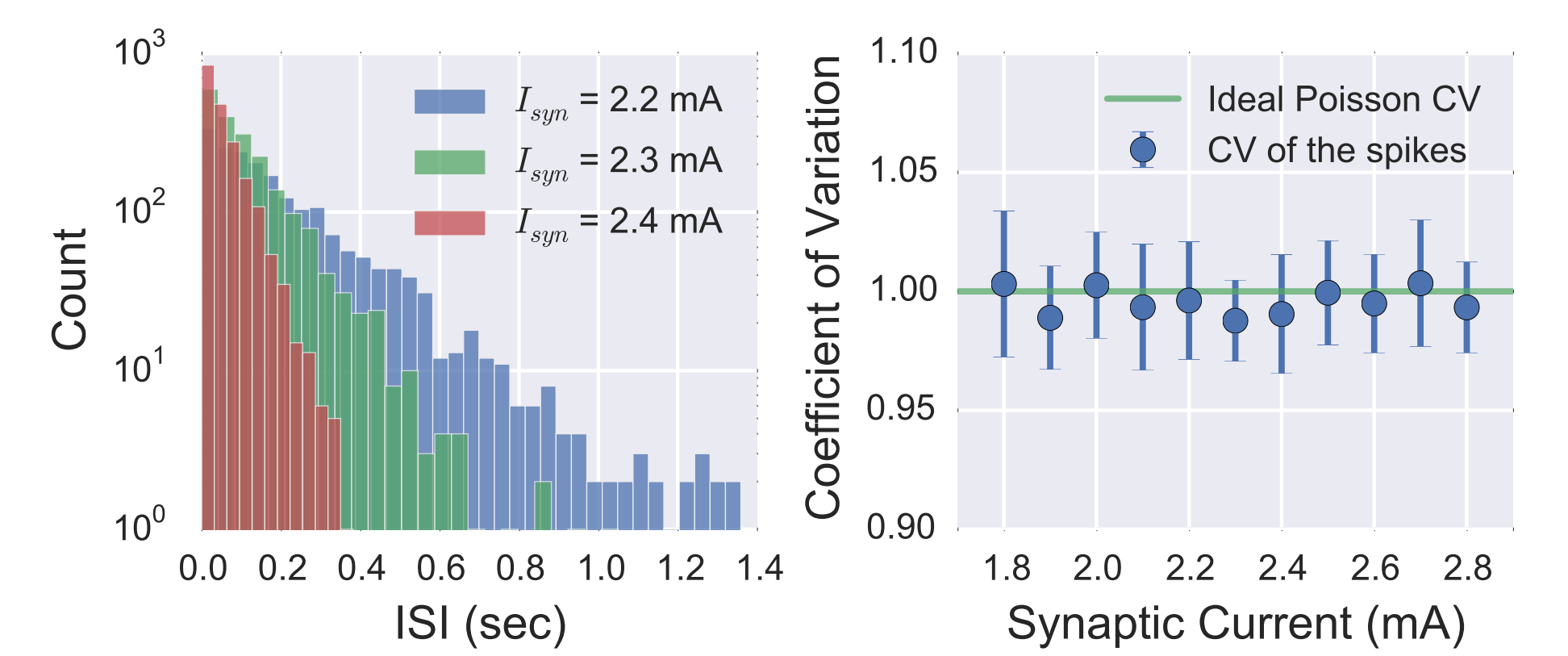


Figure 4 : The distribution of inter-spike intervals (ISI).

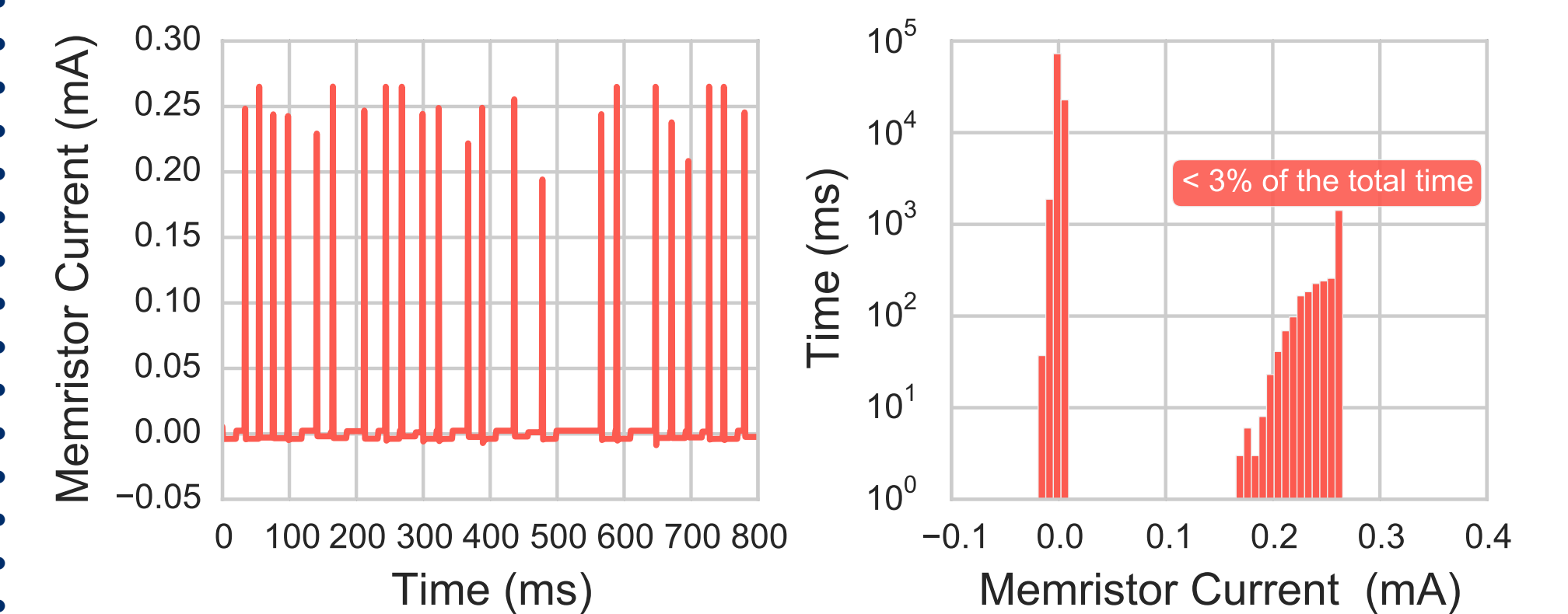


Figure 5 : Current through the memristor during spiking.

Spiking Winner-Take-All Network

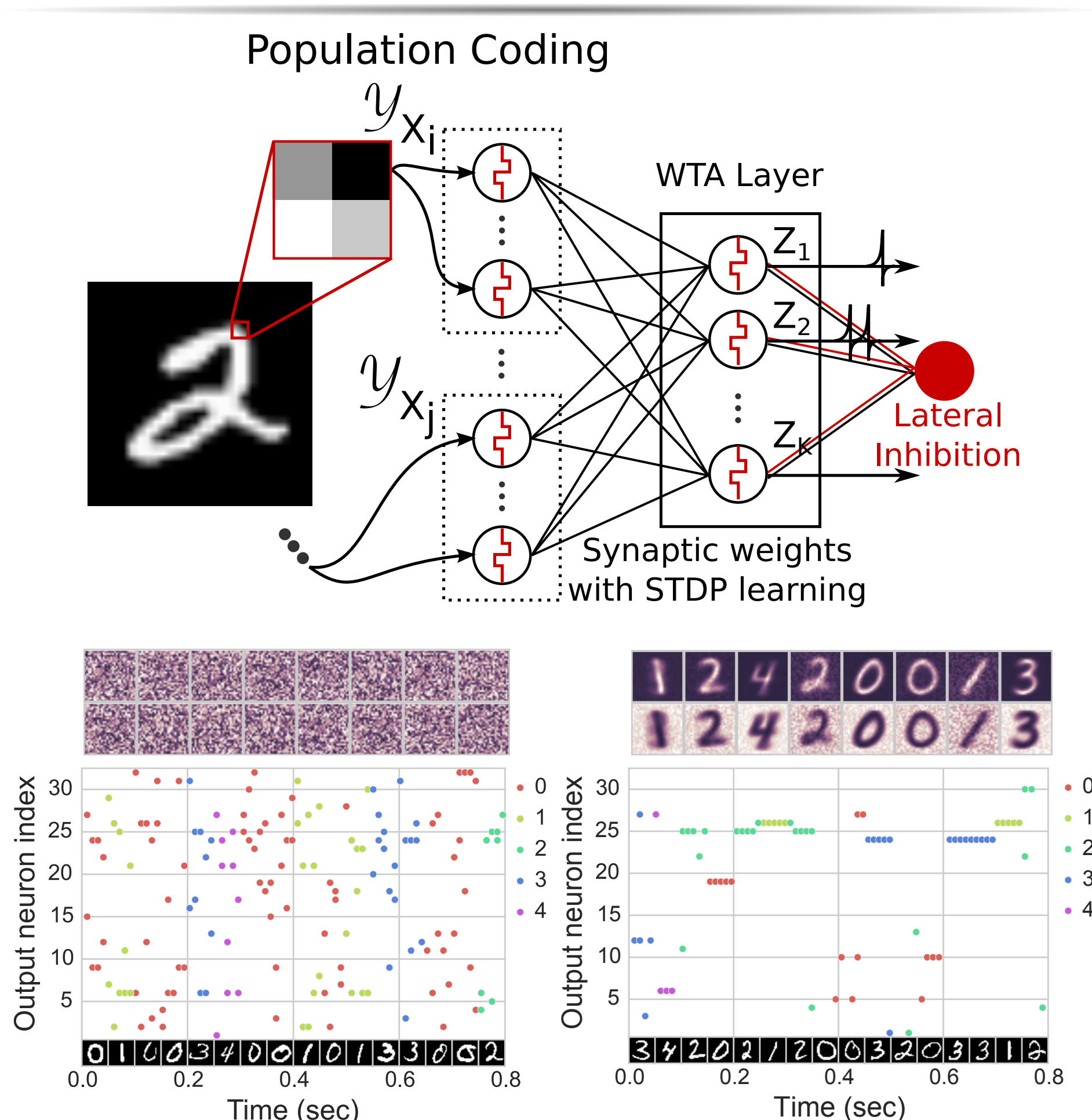
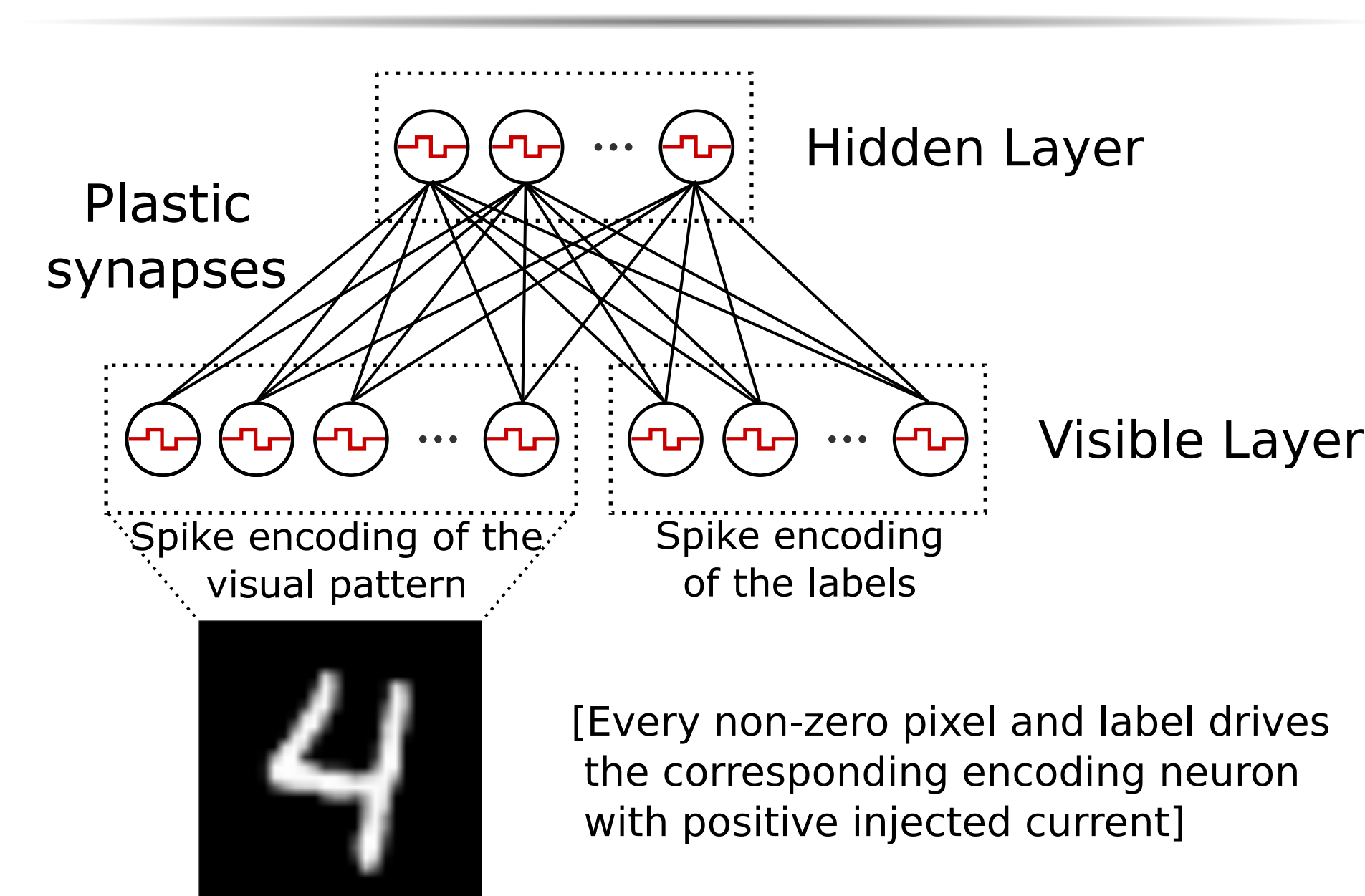


Figure 6 : Synaptic weights and WTA spiking activity.

Parameter name	Parameter value & classification accuracy			
Output layer size	16	32	64	128
Accuracy	58.9%	64.2%	73.9%	78.4%
Robustness to memristor imperfections (32 output neurons)				
Variability in τ_0	0%	20%	40%	60%
Accuracy	64.3%	64.2%	62.5%	63.0%
Variability in V_0	5%	10%	15%	20%
Accuracy	54.1%	42.0%	27.8%	16.6%

Table 1 : WTA Performance Under Different Conditions.

Spiking Boltzmann Machine



We trained an RBM and mapped its parameters onto a spiking neural network consisting of 824 visible units and 500 hidden units. The same network was capable of both discrimination (classification) and generation:

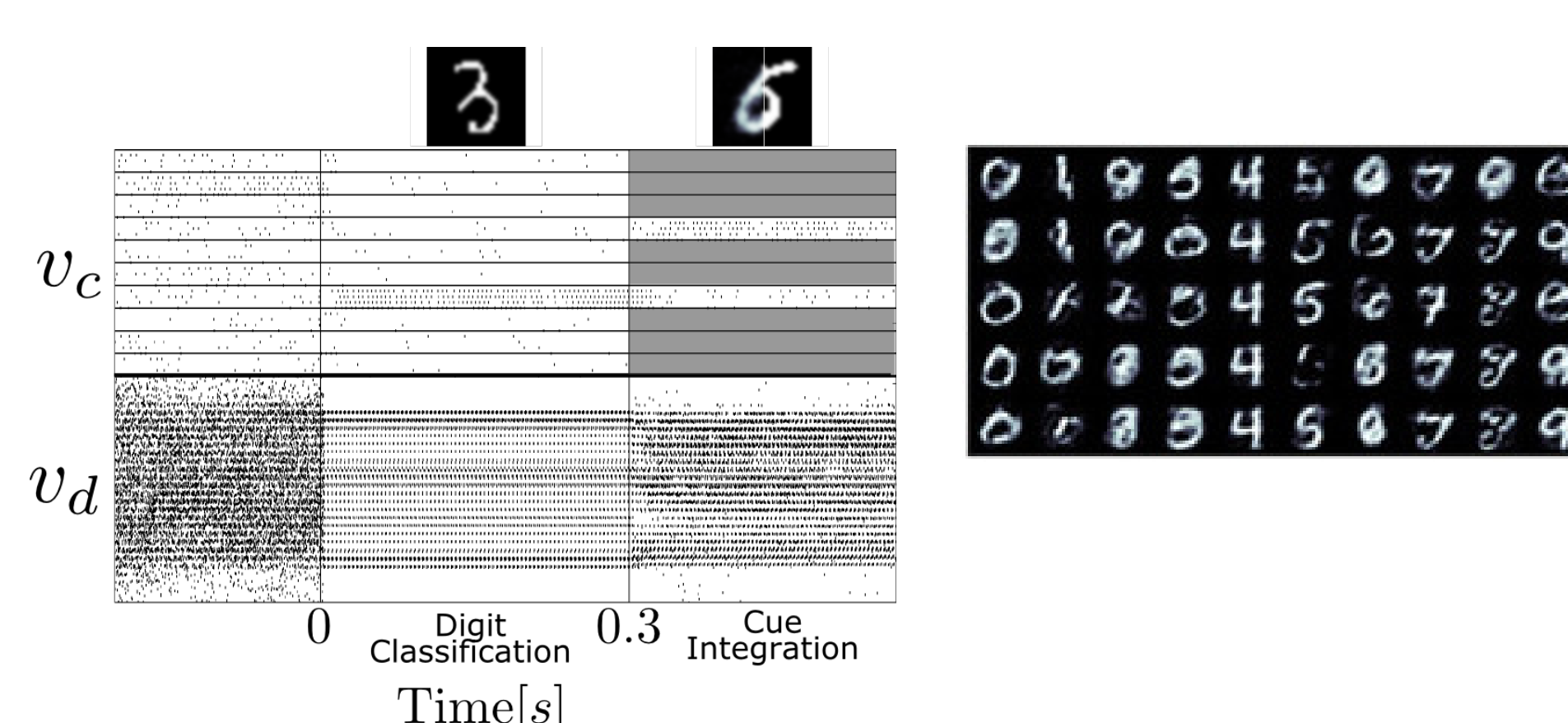


Figure 7 : Raster plot of the visible layer spiking activity in the neuromorphic RBM (classification and restricted reconstruction tasks) and the reconstructed visual patterns.

Discussion and Future Work

- The proposed memristive stochastic spiking neuron is more area- and power-efficient than the classical noise injection approach, and hence is scalable.
- Future work includes large-scale circuit-level simulations and fully memristive spiking system design.

Conclusions

- The proposed neuron is a native implementation of the stochastically firing SRM [4].
- The proposed noise generation mechanism based on memristive switching is power-efficient.
- Full compatibility with WTA and RBM networks.

References

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